

Colorboard 264/SE30

Specification

FIX 34061 REGISTER VALVES

Revision A1

June 1, 1989

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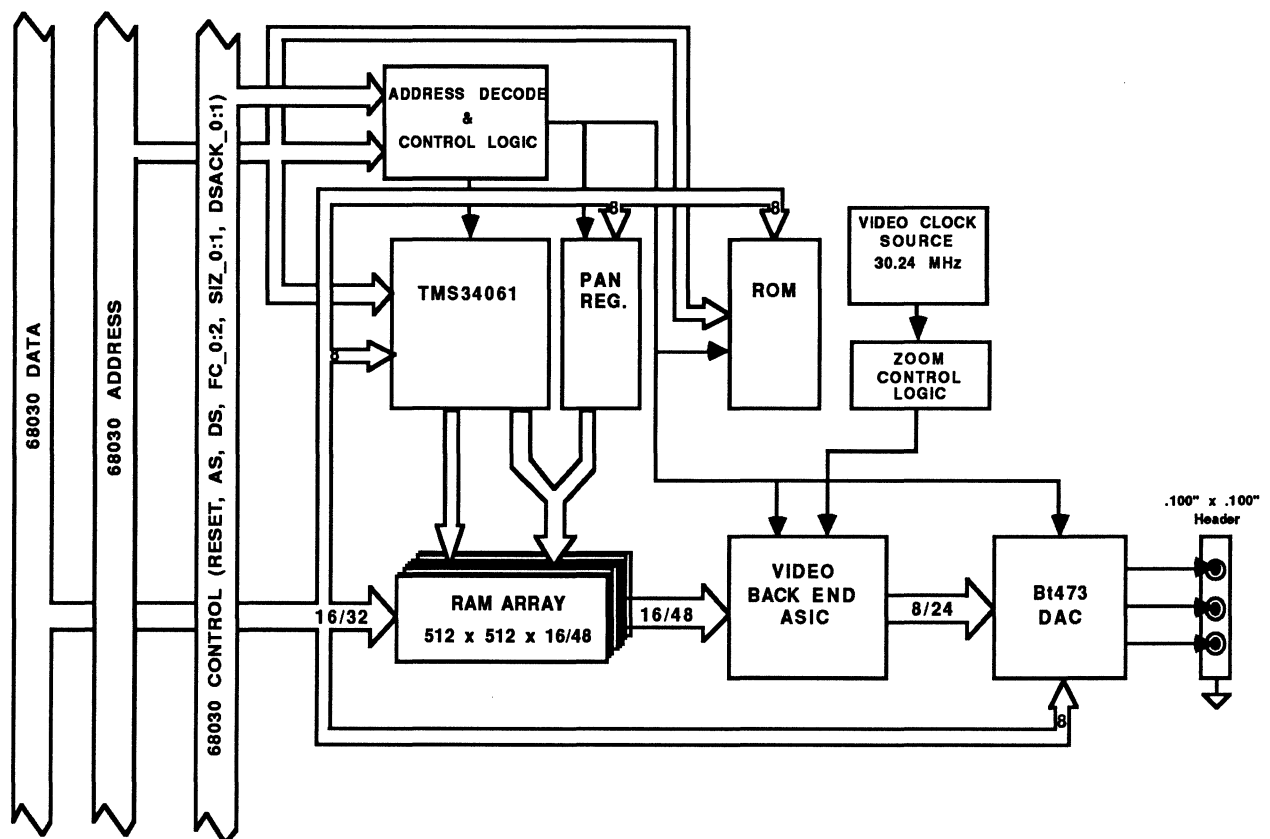
RasterOps Corporation

PART # XXXX-XXXX

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1.0 Introduction

This document establishes the physical and electrical characteristics for the Colorboard 264/SE30 system. The Colorboard 264/SE30 is a high resolution, high speed, graphics display card for the Macintosh SE/30. The Colorboard 264/SE30 occupies the '030 direct slot within the SE/30. It is capable of four pixel depths and two resolutions in it's standard configuration. With the addition of a video memory expansion option the number of pixel depths becomes five. A block diagram of the Colorboard 264/SE30 is shown in Figure 1-1. This document is the property of RasterOps Corporation and is confidential. Reproduction of this document is prohibited.



264/30 Block Diagram

Figure 1-1 Colorboard 264/SE30 Block Diagram

2.0 Hardware Description

2.1 Overview

The Colorboard 264/30's function is to provide the Macintosh SE/30 user with a low cost, versatile, high resolution frame buffer. The Colorboard 264/SE30 supports pixel depths of 1, 2, 4 and 8-bit in it's standard configuration with 24-bit becoming available with the addition of the video memory expansion option. Added features include RasterOps Virtual Screen, hardware zooming of 1X, 2X and 4X and hardware panning for full memory utilization and fast image enlargement.

2.2 Features

Switchable Standard Resolutions of

- 640 x 480
- ZZZ xYYY

64K or 256K ROM Available

Pixel Depths of 1, 2, 4, 8 and 24-bit (optional)

Occupies SE/30's '030 Direct Slot

256 Colors Displayable from a 16.7 Million Color Palette (standard)
16.7 Million Colors Displayable (with option)

35 and 48KHz Monitors Supported Standard

Current Consumption of 1.5 Amps at 5 Volts

RS-343A Compatible

15-Pin D-Subminiature Connector (Same as Apple)

Hardware Zoom of 1X, 2X, and 4X

Hardware Pan

Virtual Desktop

FCC Class B Certified
Utilizes RasterOps "Video Back End" ASIC

Separate H and V Sync Signals on the Video Connector for VGA
Compatability

3.0 Technical Data

3.1. Absolute Maximum Ratings

Supply Voltage, VCC	5.25 Volts
Operating Ambient Temperature Range	0 °C to 60 °C
Storage Temperature	-65 °C to 150 °C
ICC (Supply Current)	1.5 A @ 5.0 V

3.2 Reference Drawings

The following items should be referenced for detailed information on the Colorboard 264/SE30 system.

Colorboard 264/SE30 Top Assembly Drawing	0002-0075
Colorboard 264/SE30 Assembly	0002-0072
Colorboard 264/SE30 Schematics	0002-0071
Colorboard 264/SE30 PCB Fab	0002-0073
Colorboard 264/SE30 L/M	0002-0074

3.3 Video Specifications

3.3.3 Resolution 640 x 480 67 Hz

1 Pixel = 33.06878 nS = 30.24 MHz
1 VidClk = 529.1005 nS = 1.89 MHz
640 Pixels Horizontal Visible
864 Pixels Horizontal Total
64 Pixels Horizontal Front Porch
64 Pixels Horizontal Sync
96 Pixels Horizontal Back Porch
480 Lines Vertical Visible
525 Lines Vertical Total
3 Lines Vertical Front Porch

3 Lines Vertical Sync
39 Lines Vertical Back Porch
Horizontal Frequency = 35.0000 KHz
Vertical Frequency = 66.6666 Hz

4.0 Addressing

Because the Colorboard 264/SE30 requires more than 1 MByte of addressable space it will only run in 32-Bit mode. The 16 Megabyte memory map is shown in Figure 4-1. The 1 Megabyte sub-address map is shown in Figure 4-2.

264/30 ADDRESS MAP

16 MEGABYTE SLOT

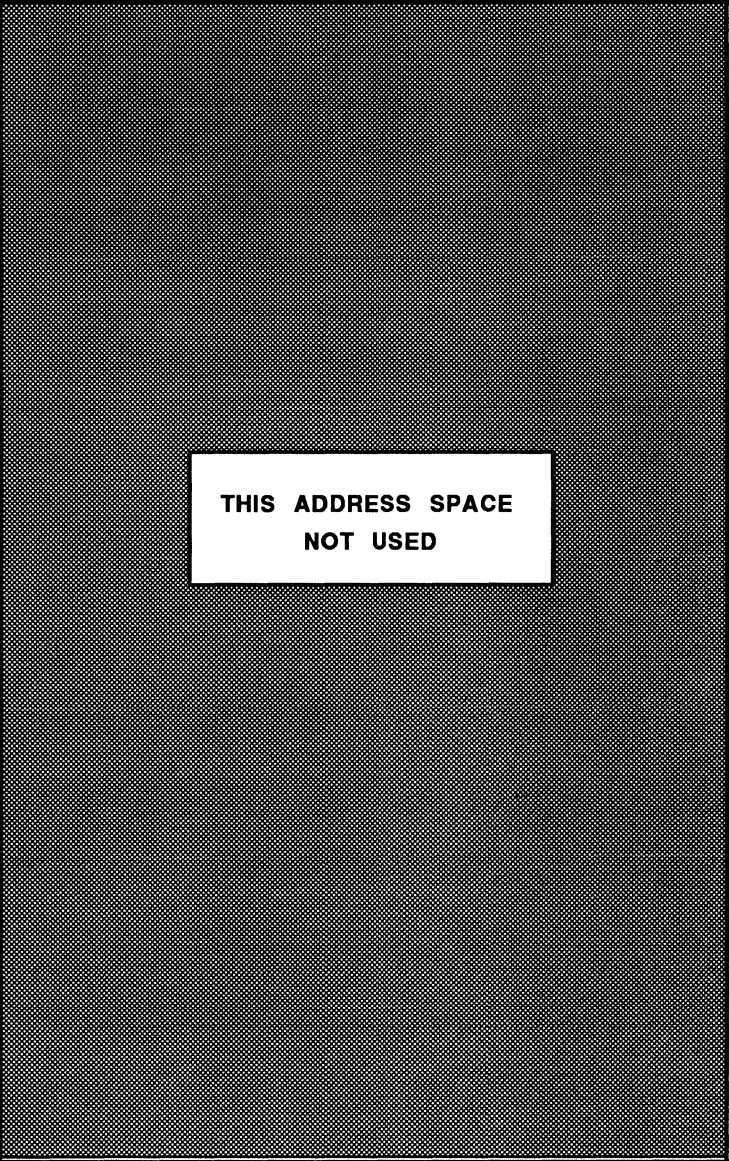
\$FBFF FFFF	TMS34061,REGISTERS,DAC AND ROM
\$FBF0 0000	
\$FBEF FFFF	
	
\$FB20 0000	1.5 MEGABYTE MEMORY OPTION
\$FB1F FFFF	
\$FB08 0000	
\$FB07 FFFF	512 KBYTES VIDEO MEMORY
\$FB00 0000	

Figure 4-1 16 Megabyte Memory Map

4.1 TMS34061 Video System Controller

A TMS34061 is used to control all the Video DRAM functions such as display update, refresh, and host direct access. The '061 has an 8-bit wide host port for access to eighteen internal 16-bit registers. These registers are used for control of the display timing and several other functions. It should be noted that not all 16 bits are utilized in each register. Register bits that are not utilized can not be programmed and are read as zeros during register read operations. The TMS34061 registers are shown in Figure 4-2.

**NOTE: X = Non-utilized bit
A = Utilized bit**

Horizontal End Sync Register

16	1211	0
X	X	X
A	A	A

Horizontal Start Blank Register

16	1211	0
X	X	X
A	A	A

Vertical End Sync Register

16	1211	0
X	X	X
A	A	A

Vertical Start Blank Register

16	1211	0
X	X	X
A	A	A

Display Update Register

16		4	3	0
X	X	X	X	X
A	A	A	A	A

Vertical Interrupt Register

16	1211	0
X	X	X
A	A	A

Control Register #2

16	5	1	4	0
X	X	X	X	X
A	A	A	A	A

X-Y Offset Register

16	1211	0
X	X	X
A	A	A

Display Address Register

16	1211	0
X	X	X
A	A	A

Horizontal End Blank Register

16	1211	0
X	X	X
A	A	A

Horizontal Total Register

16	1211	0
X	X	X
A	A	A

Vertical End Blank Register

16	1211	0
X	X	X
A	A	A

Vertical Total Register

16	1211	0
X	X	X
A	A	A

Display Start Register

16	1211	0
X	X	X
A	A	A

Control Register #1

16	5		5	4	3	0
X	A	A	A	A	A	A
X	A	A	A	A	A	A

Status Register

16		3	2	0
X	X	X	X	X
X	X	X	X	X

X-Y Address Register

16		0
A	A	A
A	A	A

Vertical Count Register

16	1211	0
X	X	X
A	A	A

Figure 4-1

Reads and writes to the TMS34061 internal registers are done one byte at a time, thus it takes two 68030 write transactions to program an entire register. The upper and lower bytes of a register correspond to two distinct addresses, making programming of the registers a straightforward process. The Colorboard 264/SE30 hardware supports only word accesses to the '061. In other words, if the 68030 accesses any portion of the Colorboard 264/SE30 with the exception of the Video Ram, the Colorboard 264/SE30 will "DSACK" the 68030 as if it were a 16 bit port. For this reason the data to be written (or read) to the '061 must appear in 68030 byte lane 0, that is data bits D31 - D24. All other data is ignored. It should also be noted that the '061 is the only interrupt source for the Colorboard 264/SE30. The addresses of the register bytes are

shown below.

<u>REGISTER NAME</u>	<u>ADDRESS</u>	<u>DESCRIPTION</u>
Horizontal End Sync Byte 0	\$FBFB 0000	This value is compared to the horizontal count and determines when horizontal sync ends.
Horizontal End Sync Byte 1	\$FBFB 0004	
Horizontal End Blank Byte 0	\$FBFB 0008	This value is compared to the horizontal count and determines when horizontal blank ends.
Horizontal End Blank Byte 1	\$FBFB 000C	
Horizontal Start Blank Byte 0	\$FBFB 0010	This value is compared to the horizontal count and determines when horizontal blank starts.
Horizontal Start Blank Byte 1	\$FBFB 0014	
Horizontal Total Byte 0	\$FBFB 0018	This value is compared to the horizontal count and determines when horizontal sync begins.
Horizontal Total Byte 1	\$FBFB 001C	
Vertical End Sync Byte 0	\$FBFB 0020	This value is compared to the vertical count and determines when vertical sync ends.
Vertical End Sync Byte 1	\$FBFB 0024	
Vertical End Blank Byte 0	\$FBFB 0028	This value is compared to the vertical count and determines when vertical blank ends.
Vertical End Blank Byte 1	\$FBFB 002C	
Vertical Start Blank Byte 0	\$FBFB 0030	This value is compared to the vertical count and determines when vertical blank starts.
Vertical Start Blank Byte 1	\$FBFB 0034	
Vertical Total Byte 0	\$FBFB 0038	This value is compared to the vertical count and determines when vertical sync begins.
Vertical Total Byte 1	\$FBFB 003C	
Display Update Byte 0	\$FBFB 0040	This value is added to the value in the Display Address Register during each horizontal blank interval.
Display Update Byte 1	\$FBFB 0044	
Display Start Byte 0	\$FBFB 0048	This value is loaded into the Display Address Register by the TMS34061 at the beginning of each vertical blank interval.
Display Start Byte 1	\$FBFB 004C	
Vertical Interrupt Byte 0	\$FBFB 0050	This value is compared to the vertical count and determines after which scan line the TMS34061 -INT output is driven to its active state.
Vertical Interrupt Byte 1	\$FBFB 0054	
Control 1 Byte 0	\$FBFB 0058	The contents of this register are explained in detail later in this section.
Control 1 Byte 1	\$FBFB 005C	
Control 2 Byte 0	\$FBFB 0060	The contents of this register are explained in detail later in this section.
Control 2 Byte 1	\$FBFB 0064	
Status Byte 0	\$FBFB 0068	The contents of this register are explained in detail later in this section.
Status Byte 1	\$FBFB 006C	

X-Y Offset Byte 0	\$FBFB 00 7B	This register is not utilized in the
X-Y Offset Byte 1	\$FBFB 00 7A	Colorboard 264/SE30.
X-Y Address Byte 0	\$FBFB 00 7C	This register is not utilized in the
X-Y Address Byte 1	\$FBFB 00 7D	Colorboard 264/SE30.
Display Address Byte 0	\$FBFB 00 7E	The contents of this register are used to
Display Address Byte 1	\$FBFB 00 7F	supply the video RAM with its row address
		during display update cycles.
Vertical Count Byte 0	\$FBFB 00 80	This register contains the value of the vertical
Vertical Count Byte 1	\$FBFB 00 81	count. This is a read-only register.

For the Colorboard 264/SE30 the X-Y Offset Register Bytes 0 & 1, the X-Y Address Register Bytes 0 & 1, the Display Update Register Byte 1, and the Status Register Byte 1 will not be utilized. Additionally, it should be noted that the Status Register and the Vertical Count Register are **READ-ONLY** registers.

Of particular interest within the TMS34061 are three registers; Control Register 1, Control Register 2, and the Status Register. A description of these registers and their contents is given below.

CONTROL REGISTER 1

BIT(S) FUNCTION

15	Reserved - always zero. When read Bit 15 returns a 0.
14 -12	RAM Refresh Burst Length. The binary value contained in these three bits determines the number of VRAM refresh cycles generated per horizontal scan line (up to 7). A value of 000 (for bits 14, 13, & 12 respectively) produces no refresh cycles, a value of 001 produces one refresh cycle per scan line, etc.
11	Error Interrupt Enable. When this bit is set to a zero , the setting of an error interrupt flag in the TMS34061 Status Register does not cause the TMS34061 to send an interrupt to the host processor. When this bit is set to a one , the setting of either the display or refresh error interrupt flag does cause an interrupt request.
10	Vertical Interrupt Enable. When this bit is set to a zero , the setting of the Vertical Interrupt flag in the Status Register does not cause an interrupt request to the processor. When this bit is set to a one , the interrupt request is enabled.
9	Interlace Enable. When this bit is set to zero , the TMS34061 is configured for non-interlaced scan. When this bit is set to a one , the TMS34061 is configured for interlaced scan.
8	External Sync Enable. When this bit is set to a zero , the external video sync mode is disabled . When this bit is set to a one , the external video sync mode is

enabled.

- 7 Display-Update RAS Mode. When this bit is set to **zero**, **all four** RAS outputs on the TMS34061 (-RAS0 to -RAS3) will be active during a display-update cycle. When this bit is set to a **one**, **only one** of the RAS outputs will be active during a display-update cycle. The active RAS output is selected by the value contained in the two most-significant *utilized* bits (bits 10 & 11) of the Display Address Register.
- 6 Display Update Direction. When this bit is set to **zero**, data is transferred from the memory cell array to the internal shift register within the VRAM during a display-update cycle. When this bit is set to a **one**, data is transferred from the internal shift register to the memory cell array during a display-update cycle.
- 5 Display Update Inhibit. When this bit is set to a **one**, the display-update cycles are **inhibited** and do not occur. When this bit is set to **zero**, the display-update cycles are **enabled**.
- 4 Reserved - always zero. When read Bit 15 returns a **0**.
- 3 - 0 Line Count Limit. The binary value contained in these four bits determines the number of horizontal scan lines that are counted by the Scan Line Counter before a display-update cycle is granted. A value of 0000 (for bits 3, 2, 1, & 0 respectively) will produce a display-update cycle after each scan line. A value of 0001 will produce a display update cycle after every other scan line. A value of 0010 will produce a display-update cycle after every third scan line, etc. The maximum value of 1111 will produce a display-update cycle after every sixteenth scan line.

CONTROL REGISTER 2

BIT(S) FUNCTION

- 15 Reserved - always zero. When read Bit 15 returns a **0**.
- 14 RAS/CAS Ready Enable. When this bit is set to **zero**, the TMS34061 output **-CASHI or -CASLO** enables the READY output timing. When this bit is set to a **one**, the operative RAS output (**-RAS3 to -RAS0**) enables the READY output timing.
- 13 Screen Enable. When this bit is set to **zero**, the TMS34061 **-BLANK** output is **active-low continuously**. When this bit is set to a **one**, the **-BLANK** output is driven low only during horizontal and vertical blanking intervals.
- 12 - 11 RDY/-HOLD Mode Select. The TMS34061 RDY/-HOLD output can be configured to operate as a "ready", "wait" or "hold" signal. The binary value of bits 12 & 11 determine which mode is selected. A value of 00 (for bits 12 & 11 respectively) selects the ready mode, a value of 01 selects the wait mode, and a value of 10 selects the hold mode. The value of 11 is reserved.
- 10 - 8 Wait State Limit. The binary value contained in these three bits determines the number of wait states inserted into host initiated read or write cycles. One wait state

is equal to one-half of a SYSCLK cycle. These wait states apply to reads and writes to the memory system controlled by the TMS34061 as well as TMS34061 internal registers. A value of 000 (for bits 10, 9, & 8 respectively) will cause no wait states to be inserted, a value of 001 will cause one wait state to be inserted, etc.

- 7 X-Y Address Pointer RAS Mode. X-Y addressing is not supported by the Colorboard 264/SE30 and, hence, the value of this bit will be inconsequential.

- 6 Extended RAS Mode. When this bit is set to **zero**, this bit will cause the values input on the TMS34061 inputs **RS0 & RS1** to select which one of the four RAS outputs will be active during a host direct cycle. When this bit is set to a **one**, this bit will cause the active RAS output to be selected by **bits 0 & 1 of Control Register 2**. The Extended RAS mode is not utilized by the Colorboard 264/SE30 and, hence, the value of this bit should be kept at zero.

- 5 - 2 RAS Overrides. Each of these four bits is dedicated to one of the four TMS34061 RAS outputs (-RAS3 to -RAS0). When an override bit is set to **one**, the corresponding RAS output is **forced to its active-low state** during host-direct write cycles, X-Y indirect write cycles, shift-register write cycles, and shift-register read cycles. When an override bit is set to **zero**, the corresponding RAS output is **controlled by other means**. The RAS override function is not utilized by the Colorboard 264/SE30, hence, bits 5 through 2 should be kept at zero.

- 1 - 0 Extended RAS Select Bits. When bit 6 of Control Register 2 is a one, bits 1 & 0 select which of the four TMS34061 RAS outputs will be driven active during host-direct cycles. A value of 00 (for bits 1 & 0 respectively) selects the -RAS0 output, a value of 01 selects the -RAS1 output, a value of 10 selects the -RAS2 output, and a value of 11 selects the -RAS3 output. The Extended RAS mode is not utilized by the Colorboard 264/SE30 and, hence, the value of these bits will be inconsequential.

STATUS REGISTER

BIT(S) FUNCTION

- 15 - 3 These bits are not utilized. When read Bits 15 through 3 return a **0**.

- 2 Refresh Error. A one in this bit indicates that the TMS34061 was unable to execute the designated number of VRAM refresh cycles before the beginning of the next horizontal blanking interval.

- 1 Display Error. A one in this bit indicates that the TMS34061 was unable to perform a display-update cycle requested during the horizontal blanking interval.

- 0 Vertical Interrupt. A one in this bit indicates that the vertical interrupt condition has occurred.

If any of bits 2 through 0 in the Status Register are set to one, the TMS34061 will drive its -INT output active low. This will, in turn, cause an interrupt to be generated to

the host processor. A read of the Status Register will clear bits 2 through 0. This will cause the TMS34061 -INT output to be driven to its inactive high state, thus cancelling the interrupt to the host processor.

4.2 The Video RAM

The Colorboard 264/SE30 contains 512 Kbytes of dual port RAM in it's standard configuration. In this configuration the Colorboard 264/SE30 is limited to operate in 1-bit, 2-bit, 4-bit or 8-bit mode. Also, in this configuration the data path to the Video Ram is 16 bits wide. Therefore, when the 68030 accesses the Video Ram, the Colorboard 264/SE30 will **"DSACK"** the 68030 as if it were a 16 bit port. The data stored in the Video Ram can be read or written on a byte or word basis only. However, since the 68030 utilizes dynamic bus sizing this should be transparent to software. The video RAM may be read from or written to over 68030 byte lanes 0 and 1 (data bits D31-D24). The address range of the video RAM is **\$FB00 0000 through \$FB07 FFFF**.

The Colorboard 264/SE30 can be upgraded to contain a full 1.5 Megabytes of video memory. In this configuration the Colorboard 264/SE30 can operate in 1, 2, 4, 8, or 24-bit mode. For this configuration the data path to the Video Ram is 24 bits wide. Therefore, when the 68030 accesses the Video Ram, the Colorboard 264/SE30 will **"DSACK"** the 68030 as if it were a 32 bit port. The data stored in the Video Ram can be read or written on a longword basis only. The video RAM may be read from or written to over 68030 byte lanes 1, 2 and 3 (data bits D23-D0). The address range of the video RAM is **\$FB00 0000 through \$FB0F FFFF**.

4.3 The Mode Register

The Colorboard 264/SE30 contains one 12 bit Mode Register used for storing both status and control information. Although all twelve bits of this register may be read by the host, only the most significant eight bits may be programmed. Reading from or writing to the register is done over 68030 byte lanes 0 and 1 (data bits D31-D20). It should be noted that the most significant eight bits of the Mode Register are reset to logical zeros during reset. Therefore the Colorboard 264/SE30 initialization routine should include the appropriate reprogramming of these bits. The contents of the Mode Register and its address are shown below.

MODE REGISTER (ADDRESS \$FBFD 0000)

<u>BIT(S)</u>	<u>FUNCTION</u>
7 15	Not Used.

6 - 10

Not Used.

5-4 - 9-8

ZOOM1 and ZOOM0. These bits control the zoom amount in the X-direction. Their decoding is shown below.

BIT9/BIT8ZOOM FACTOR

00
01
10
11

1X
2X
4X
NOT USED

3 - 7

OSCSEL. This bit is used to determine the video output. When this bit is a **zero** the Colorboard 264/SE30 will output video at xxx x xxx resolution with a 12.5 pixel frequency (**Apple's xx" Interlaced RGB monitor**). When this bit is a **one** the Colorboard 264/SE30 will output video at 640 x 480 resolution with a 30.24 MHz pixel frequency (**Apple's 15" non-interlaced RGB monitor**).

2 - 6 - 64

+CHUNKY, MODE1 and MODE0. These bits are used to select the pixel depth that the Colorboard 264/SE30 will operate in. Their decodings are shown below.

BIT6/BIT5/BIT4PIXEL DEPTH

000
001
010
011
100
101
110
111

1-BIT
2-BIT
4-BIT
8-BIT
NOT ALLOWED
NOT ALLOWED
NOT ALLOWED
24-BIT

3 -

~~MONITOR. This bit is used to identify the presence of an external monitor. When this bit is a zero it signifies that an external monitor is connected to the Colorboard 264/SE30. When this bit is a one it signifies that there is not an external monitor connected to the Colorboard 264/SE30.~~

~~MONITOR = 0 640 x 480 60 HZ~~

~~MONITOR = 1 * 640 x 480 30 HZ INTERLACED BV SCAN~~

2 -

-OPTION. This bit is used to identify the presence of the extended video RAM option on the Colorboard 264/SE30. When this bit is a **zero** it signifies that **1.5 MBytes of video memory** are available for use (and 24-bit mode is allowed). When this bit is a **one** it signifies that only **512 KBytes of video memory** are available on the Colorboard 264/SE30 (only 1, 2, 4 and 8-bit modes are allowed).

1 -

Not Used.

0 -

Not Used.

* 556 x 416 UNDERSCAN

4.4 The Pan Register

The Colorboard 264/SE30 contains one 9 bit Pan Register used for storing the X coordinate of a video pan (this X coordinate translates directly into a column address for the video RAM). All nine bits of the Pan Register may be read from or written to over the 68030 byte lanes 0 and 1 (data bits D31-D23). It should be noted that there is a limited range of values that may be programmed into the Pan Register for proper operation. The range of values and the values themselves depend on the choice of "color" and resolution modes at the time the Pan Register is programmed. The address of the Pan Register is **\$FBFC 0000**.

4.5 The Bt473 DAC

The Brooktree Bt473 contains several internal programmable devices. These devices include; three internal 256 x 8 bit color lookup tables (CLUTs) within which is stored the DAC color data, three sets of fifteen 8 bit Overlay Registers used for overlaying information (i.e. cursors, text, etc.) on existing video, one 8 bit Address Register used for specifying the location within the CLUT or the Overlay Register which is to be read from or written to, one 8 bit Command Register used for certain DAC controls and one 8 bit Pixel Read Mask Register. The three sets of fifteen overlay registers will not be used by the Colorboard 264/SE30 and, hence, are excluded from this discussion. Writes to and reads from any device within the Bt473 are done one byte at a time over 68030 byte lane 0 (data bits D31-D24).

Each of the three sets of 256 CLUT locations contains one byte of data for each of the red, green and blue Digital-to-Analog converters (24 bits total). A write to a location within the CLUT is done in the following manner; the address of the CLUT location to be programmed (\$00h to \$FFh) is written into the Bt473 Address Register. Three consecutive byte writes are then done to the CLUT. The first byte contains the data for the red DAC, the second byte contains the data for the green DAC and the third byte contains the data for the blue DAC. At the end of the third (blue) byte's write cycle the value contained in the CLUT Address Register is incremented, thus pointing to the next CLUT location. It should be noted that the Address Register wraps around such that when three bytes are written to the CLUT when the value in the Address Register is \$FFh, the Address Register will "increment" to point at CLUT location \$00h. It can be seen that programing the Address Register once will allow for all locations within the CLUT to be accessed.

A read of a CLUT location is very similar to a write; the address of the CLUT location is loaded into the Address Register and three consecutive reads are performed. The first read will yield the byte containing the red DAC data, the second read will yield the byte containing the green DAC data and the third read will yield the byte containing the blue DAC data. Similar to a write, at the end of the third byte's read cycle, the value in the Address Register is incremented, thus pointing to the next CLUT location. Address Register wrap around applies to reads as well as writes.

It should be noted that there are actually four addresses assigned to the Bt473 Address Register. These addresses correspond to; a CLUT read, a CLUT write, an Overlay Register read, and an Overlay Register write. Addresses for the Bt473 internal devices are given below.

<u>REGISTER NAME</u>	<u>ADDRESS</u>
Address Register (RAM write mode)	\$FBFE 0000
Address Register (RAM read mode)	\$FBFE 0006
Address Register (Overlay write mode)	\$FBFE 0008
Address Register (Overlay read mode)	\$FBFE 000E
Pixel Read Mask Register	\$FBFE 0004
Color Palette RAM	\$FBFE 0002
Overlay Registers	\$FBFE 000A
Command Register	\$FBFE 000C

The contents of the 8-bit Pixel Read Mask Register are bit-wise logically ANDED with the byte input to the Bt473 which specifies the CLUT location which is to be used for the current pixel. For the Colorboard 264/SE30 the contents of the Pixel Read Mask Register should always be set to \$FF.

Of special interest within the Bt473 is the Command Register. The Command Register is used to control some of the special functions of the Bt473. A complete description of the Command Register is given below. It should be noted that the Command Register attains no default value after reset and therefore must be programmed before the Colorboard 264/30 will operate properly.

DAC COMMAND REGISTER (ADDRESS \$FBFE 000C)

<u>BIT(S)</u>	<u>FUNCTION</u>
----------------------	------------------------

- | | |
|-----|--|
| 7-6 | Color Mode Select Bits. These bits are used to control the various color modes of the Bt473 DAC. They are used in conjunction with two external inputs to the Bt473 to select which pixel inputs are used and what the selected pixel inputs are used for. For a comprehensive discussion on the use of these bits consult the Brooktree databook. |
| 5 | Setup Select bit. This bit is used to specify the level of the blanking pedestal. When this bit is a zero it specifies a 0 IRE blanking pedestal. When this bit is a one it specifies a 7.5 IRE blanking pedestal. |

- 4 DAC Pixel Depth Select. This bit specifies whether the Bt473 is to operate in 8-bit per pixel mode or 6-bit per pixel mode. When this bit is a **zero** it specifies that the DAC is to operate in **6-bit per pixel** mode. When this bit is a **one** it specifies that the DAC is to operate in **8-bit per pixel** mode.
- 3-0 Not Used.

4.7 The Configuration ROM

The Configuration ROM consists of a 27C64-250 or 27C256-250 EPROM IC physically wired to the 68030 byte lane 0 (data bits D31-D24). The Configuration ROM must have a value of ??(hex) at location \$FBFF FF?? (27C64 ROM, byte read) or \$FBFF FF?? (27C256 ROM, byte read). In addition, other header information must be included in the Configuration ROM for the slot manager to function properly. See chapter 8 of the Macintosh II Specification for more details on this topic.

The Configuration ROM is 8-bits wide (one byte), the data always appears in 68030 byte number 3 and any type of read access is allowed (byte, word, long-word).

The configuration ROM contains a primary initialization, Apple compatible video driver, slot manager and video resources for all modes in 640 x 480 resolutions. The primary initialization, when executed by the slot manager, initializes the DAC, 34061 registers, mode register and gray wipes the screen.

5.0 Programming the Colorboard 264/SE30

5.1 Standard Usage

The following are lists of values that need to be programmed into the various registers of the Colorboard 264/SE30 to insure proper operation in all modes. It should be noted that these values will invoke a zoom of 1X.

640 x 480 Resolution

<u>ADDRESS</u>	<u>DATA</u>	<u>COMMENTS</u>
\$FBFB 0000	\$FB 00 07 14	Horizontal End Sync Byte 0
\$FBFB 0002	\$00 00	Horizontal End Sync Byte 1
\$FBFB 0004	\$FB 00 13 80	Horizontal End Blank Byte 0
\$FBFB 0006	\$00 00	Horizontal End Blank Byte 1
\$FBFB 0008	\$FB 00 03 C0	Horizontal Start Blank Byte 0
\$FBFB 000A	\$00 00	Horizontal Start Blank Byte 1
\$FBFB 000C	\$FB 00 03 C3	Horizontal Total Byte 0
\$FBFB 000E	\$00 00	Horizontal Total Byte 1

\$FBFB 0010	\$02	02	Vertical End Sync Byte 0
\$FBFB 0012	\$00	00	Vertical End Sync Byte 1
\$FBFB 0014	\$29	13	Vertical End Blank Byte 0
\$FBFB 0016	\$00	00	Vertical End Blank Byte 1
\$FBFB 0018	\$09	03	Vertical Start Blank Byte 0
\$FBFB 001A	\$02	01	Vertical Start Blank Byte 1
\$FBFB 001C	\$0C	06	Vertical Total Byte 0
\$FBFB 001E	\$02	01	Vertical Total Byte 1
\$FBFB 0020	\$04		Display Update Byte 0
\$FBFB 0022	\$00		Display Update Byte 1
\$FBFB 0024	\$00		Display Start Byte 0
\$FBFB 0026	\$00		Display Start Byte 1
\$FBFB 0028	\$00		Vertical Interrupt Byte 0
\$FBFB 002A	\$00		Vertical Interrupt Byte 1
\$FBFB 002C	\$80	80	Control Register 1 Byte 0
\$FBFB 002E	\$74	76	Control Register 1 Byte 1
\$FBFB 0030	\$00		Control Register 2 Byte 0
\$FBFB 0032	\$68		Control Register 2 Byte 1
\$FBFD 0000	\$080		Mode Register (1-Bit Mode)
	\$0A0		" (2-Bit Mode)
	\$090		" (4-Bit Mode)
	\$0B0		" (8-Bit Mode)
	\$0F0		" (24-Bit Mode)
\$FBFE 0004	\$FF		DAC Pixel Read Mask Register
\$FBFE 000C	\$30		DAC Command Register

Additionally, the color lookup table of the Bt473 DAC needs to be loaded with the appropriate values to match the pixel depth.

5.2 Zoom and Pan

The Colorboard 264/SE30 is capable of zooming a screened image by 1X, 2X and 4X. In 1X zoom mode the entire image is always displayed on the screen and, hence, there is no need for panning unless the extended desktop function is enabled. However, in 2X zoom mode only one quarter of the entire image can be displayed at any one time and in 4X zoom mode only one sixteenth of the entire image can be displayed at any one time. Thus, in these last two modes it will be necessary to implement panning.

Zooming an image is accomplished through two separate operations; zooming in the X direction and zooming in the Y direction. X direction zooms are controlled by the Mode Register bits 9 & 8. Y direction zooms are controlled by the TMS34061's

Display Update Register byte 0. Zomming by 1X, 2X or 4X can be accomplished by loading the appropriate values into these registers. These values are shown below.

1X ZOOM

Mode Register (Address = \$FBFD 0000) = XX00XXXXXXXXb

Display Update Register byte 0 (Address = \$FBFB 0020) = XXXX0100b

2X ZOOM

Mode Register (Address = \$FBFD 0000) = XX01XXXXXXXXb

Display Update Register byte 0 (Address = \$FBFB 0020) = XXXX0010b

4X ZOOM

Mode Register (Address = \$FBFD 0000) = XX10XXXXXXXXb

Display Update Register byte 0 (Address = \$FBFB 0020) = XXXX0001b

Panning, like zooming, is also accomplished through two seperate steps; panning in the X direction and panning in the Y direction. X direction panning is controlled by the Pan Register. Y direction panning is controlled by the TMS34061's Display Start Register bytes 0 & 1. Panning is done by loading appropriate values into these registers.

Granularity of panning in the X direction is dependent upon the pixel mode. In one bit per pixel mode the minimum distance one can pan is 16 pixels. In two bit per pixel mode, the minimum X direction pan is 8 pixels. In four bit per pixel mode, the minimum X direction pan is 4 pixels. And, finally, in eight bit per pixel mode, the minimum X direction pan is 2 pixels. Regardless of the pixel mode, the minimum Y direction pan distance is always one pixel.

Panning can be utilized to display any part of a zoomed image on the screen. There are, however, maximum values that should be loaded into the Pan and Display Start Registers to prevent panning beyond the image. Additionally, it may be convenient to pan around a zoomed image one full screen at a time. The maximum and full screen values are given below.

1	2
3	4

2X ZOOM

1	2	3	4
5	6	7	8
9	10	11	12
13	14	15	16

4X ZOOM

Pan Register Address = \$FBFC 0000

Display Start Register Address = \$FBFB 0024 (Byte 0) & \$FBFB 0026 (Byte 1)

Resolution = 640 x 480

8-Bit Mode, 2X Zoom

Pan Register

Screen 1	\$00,(\$00),[\$00]
Screen 2	\$80,(\$64),[\$50]
Screen 3	\$00,(\$00),[\$00]
Screen 4	\$80,(\$64),[\$50]

Display Start Register

(Byte 1, Byte 0)

\$000,(\$000),[\$000]
\$000,(\$000),[\$000]
\$600,(\$4B0),[\$3C0]
\$600,(\$4B0),[\$3C0]

8-Bit Mode, 4X Zoom

Pan Register

Screen 1	\$00,(\$00),[\$00]
Screen 2	\$40,(\$32),[\$28]
Screen 3	\$80,(\$64),[\$50]
Screen 4	\$C0,(\$96),[\$78]
Screen 5	\$00,(\$00),[\$00]
Screen 6	\$40,(\$32),[\$28]
Screen 7	\$80,(\$64),[\$50]
Screen 8	\$C0,(\$96),[\$78]
Screen 9	\$00,(\$00),[\$00]
Screen 10	\$40,(\$32),[\$28]
Screen 11	\$80,(\$64),[\$50]
Screen 12	\$C0,(\$96),[\$78]
Screen 13	\$00,(\$00),[\$00]
Screen 14	\$40,(\$32),[\$28]

Display Start Register

(Byte 1, Byte 0)

\$000,(\$000),[\$000]
\$000,(\$000),[\$000]
\$000,(\$000),[\$000]
\$000,(\$000),[\$000]
\$300,(\$270),[\$1E0]
\$300,(\$270),[\$1E0]
\$300,(\$270),[\$1E0]
\$300,(\$270),[\$1E0]
\$600,(\$4B0),[\$3C0]
\$600,(\$4B0),[\$3C0]
\$600,(\$4B0),[\$3C0]
\$600,(\$4B0),[\$3C0]
\$900,(\$708),[\$5A0]
\$900,(\$708),[\$5A0]

Screen 15	\$80,(\$64),[\$50]	\$900,(\$708),[\$5A0]
Screen 16	\$C0,(\$96),[\$78]	\$900,(\$708),[\$5A0]

4-Bit Mode, 2X Zoom

Screen 1	\$00,(\$00),[\$00]	\$000,(\$000),[\$000]
Screen 2	\$40,(\$32),[\$28]	\$000,(\$000),[\$000]
Screen 3	\$00,(\$00),[\$00]	\$600,(\$4B0),[\$3C0]
Screen 4	\$40,(\$32),[\$28]	\$600,(\$4B0),[\$3C0]

4-Bit Mode, 4X Zoom

Screen 1	\$00,(\$00),[\$00]	\$000,(\$000),[\$000]
Screen 2	\$20,(\$19),[\$14]	\$000,(\$000),[\$000]
Screen 3	\$40,(\$32),[\$28]	\$000,(\$000),[\$000]
Screen 4	\$60,(\$46),[\$3C]	\$000,(\$000),[\$000]
Screen 5	\$00,(\$00),[\$00]	\$300,(\$270),[\$1E0]
Screen 6	\$20,(\$19),[\$14]	\$300,(\$270),[\$1E0]
Screen 7	\$40,(\$32),[\$28]	\$300,(\$270),[\$1E0]
Screen 8	\$60,(\$46),[\$3C]	\$300,(\$270),[\$1E0]
Screen 9	\$00,(\$00),[\$00]	\$600,(\$4B0),[\$3C0]
Screen 10	\$20,(\$19),[\$14]	\$600,(\$4B0),[\$3C0]
Screen 11	\$40,(\$32),[\$28]	\$600,(\$4B0),[\$3C0]
Screen 12	\$60,(\$46),[\$3C]	\$600,(\$4B0),[\$3C0]
Screen 13	\$00,(\$00),[\$00]	\$900,(\$708),[\$5A0]
Screen 14	\$20,(\$19),[\$14]	\$900,(\$708),[\$5A0]
Screen 15	\$40,(\$32),[\$28]	\$900,(\$708),[\$5A0]
Screen 16	\$60,(\$46),[\$3C]	\$900,(\$708),[\$5A0]

2-Bit Mode, 2X Zoom

Screen 1	\$00,(\$00),[\$00]	\$000,(\$000),[\$000]
Screen 2	\$20,(\$19),[\$14]	\$000,(\$000),[\$000]
Screen 3	\$00,(\$00),[\$00]	\$600,(\$4B0),[\$3C0]
Screen 4	\$20,(\$19),[\$14]	\$600,(\$4B0),[\$3C0]

2-Bit Mode, 4X Zoom

Screen 1	\$00,(\$00),[\$00]	\$000,(\$000),[\$000]
Screen 2	\$10,(\$0C),[\$0A]	\$000,(\$000),[\$000]
Screen 3	\$20,(\$19),[\$14]	\$000,(\$000),[\$000]
Screen 4	\$30,(\$25),[\$1E]	\$000,(\$000),[\$000]
Screen 5	\$00,(\$00),[\$00]	\$300,(\$270),[\$1E0]
Screen 6	\$10,(\$0C),[\$0A]	\$300,(\$270),[\$1E0]
Screen 7	\$20,(\$19),[\$14]	\$300,(\$270),[\$1E0]
Screen 8	\$30,(\$25),[\$1E]	\$300,(\$270),[\$1E0]
Screen 9	\$00,(\$00),[\$00]	\$600,(\$4B0),[\$3C0]
Screen 10	\$10,(\$0C),[\$0A]	\$600,(\$4B0),[\$3C0]
Screen 11	\$20,(\$19),[\$14]	\$600,(\$4B0),[\$3C0]
Screen 12	\$30,(\$25),[\$1E]	\$600,(\$4B0),[\$3C0]
Screen 13	\$00,(\$00),[\$00]	\$900,(\$708),[\$5A0]

Screen 14	\$10,(\$0C),[\$0A]	\$900,(\$708),[\$5A0]
Screen 15	\$20,(\$19),[\$14]	\$900,(\$708),[\$5A0]
Screen 16	\$30,(\$25),[\$1E]	\$900,(\$708),[\$5A0]

1-Bit Mode, 2X Zoom

Screen 1	\$00,(\$00),[\$00]	\$000,(\$000),[\$000]
Screen 2	\$10,(\$0C),[\$0A]	\$000,(\$000),[\$000]
Screen 3	\$00,(\$00),[\$00]	\$600,(\$4B0),[\$3C0]
Screen 4	\$10,(\$0C),[\$0A]	\$600,(\$4B0),[\$3C0]

1-Bit Mode, 4X Zoom

Screen 1	\$00,(\$00),[\$00]	\$000,(\$000),[\$000]
Screen 2	\$08,(\$06),[\$05]	\$000,(\$000),[\$000]
Screen 3	\$10,(\$0C),[\$0A]	\$000,(\$000),[\$000]
Screen 4	\$18,(\$12),[\$0F]	\$000,(\$000),[\$000]
Screen 5	\$00,(\$00),[\$00]	\$300,(\$270),[\$1E0]
Screen 6	\$08,(\$06),[\$05]	\$300,(\$270),[\$1E0]
Screen 7	\$10,(\$0C),[\$0A]	\$300,(\$270),[\$1E0]
Screen 8	\$18,(\$12),[\$0F]	\$300,(\$270),[\$1E0]
Screen 9	\$00,(\$00),[\$00]	\$600,(\$4B0),[\$3C0]
Screen 10	\$08,(\$06),[\$05]	\$600,(\$4B0),[\$3C0]
Screen 11	\$10,(\$0C),[\$0A]	\$600,(\$4B0),[\$3C0]
Screen 12	\$18,(\$12),[\$0F]	\$600,(\$4B0),[\$3C0]
Screen 13	\$00,(\$00),[\$00]	\$900,(\$708),[\$5A0]
Screen 14	\$08,(\$06),[\$05]	\$900,(\$708),[\$5A0]
Screen 15	\$10,(\$0C),[\$0A]	\$900,(\$708),[\$5A0]
Screen 16	\$18,(\$12),[\$0F]	\$900,(\$708),[\$5A0]

6.0 Apple Board Identification

The Colorboard 264/SE30 is registered with Apple and has been assigned the following identifiers, which are reflected in the appropriate slot manager resources.

Board ID for ColorBoard Colorboard 264/SE30 is \$01B1.

Functional sResource ID for ColorBoard Colorboard 264/SE30 is \$0132.

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7.0 Frame Buffer

The frame buffer is designed to be accessible as a Virtual Desktop. This means that as the pixel bit depths decrease there is more memory available for storage of more pixels. The frame buffer is 1024 x 512. The maximum screen resolution is 640 x 480. Thus, the user will be able to pan in 24-bit or 8-bit mode if the Virtual Desktop feature is being utilized. In 4-bit mode the virtual screen is 2048 x 512, in 2 bit mode it is 4096 x 512, and in 1-bit mode it is 8192 x 512. The user can disable the Virtual Desktop feature via the control panel CDEV. When this is done panning can only be accomplished when the display is zoomed.

8.0 Attachments

The Colorboard 264/SE30 contains the RasterOps ASIC known as the Video Backend Controller. A copy of the Video Backend Controller specification has been attached to this specification for reference.